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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/661,502	09/15/2003	Ching-Tung Wang	TAIW 168	7402

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RABIN & CHAMPAGNE, P.C.
Suite 500
1101 14 Street, N.W.
Washington, DC 20005

EXAMINER
BODDIE, WILLIAM

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 02/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/661,502	WANG ET AL.	
	Examiner	Art Unit	
	William Boddie	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☒ Claim(s) *9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Method of Controlling a Liquid Crystal Display Data Clock to Conserve Power.

Claim Objections

2. Claim 9 is objected to because of the following informalities: on line 9 of claim 9, "drived" should be "driven". Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. Claims 1-15 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 1, 2 and 9 state a LOAD signal drives a timing controller and a DSTH signal drives a source driver. However, Applicant's disclosure seems to discuss the opposite. The disclosure states, "a DSTH signal determines the programming time of a timing controller. A LOAD signal confirms the programming time of the data into the display panel" (page 3, lines 15-16). Also contradictory to the claims is page 4, lines 3-4, "The DSTH signal controls the data input to the timing controller. The LOAD signal controls the data input to the display panel."

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3, 5-6, 8-10, 12-13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's own Prior Art admissions (hereafter APA) in view of Kim (US 6,414,670).

With respect to claim 1, APA discloses a method of driving a liquid crystal display device, the liquid crystal display device comprising driver circuit, which comprises a timing controller (110 in fig. 1) driven by a data transmission signal (LOAD signal) (fig. 2) and a source driver (120 in fig. 1) driven by a data reception signal (DSTH signal) (fig. 2).

APA does not expressly disclose, the method comprising the steps of: detecting a status of the LOAD signal; and controlling a DCLK signal (clk1 in fig. 9) according to the status of the LOAD signal (col. 5, line 33-35).

Kim discloses, detecting a status of the LOAD signal (STV2 in fig. 8); and controlling a DCLK signal (clk1 in fig. 9) according to the status of the LOAD signal (col. 5, line 33-35, col. 6, lines 3-5; also note the waveforms in fig. 9 which demonstrate a turning off of clk1).

The APA and Kim are analogous art because they are from the same field of endeavor, namely LCD control circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to only provide clock signals to the source drivers, taught by APA, which are providing driving signals to the source lines as taught by Kim. In other words, APA teaches the signals of the claimed invention. Kim teaches, based on the state of two signals, enabling or disabling a clock signal. It seems obvious that one would combine these two teachings to enable or disable the clock signal of Applicant's admitted prior art.

The motivation for doing so would have been to reduce unnecessary power consumption (Kim, col. 6, lines 3-5).

Therefore it would have been obvious to combine Kim with APA for the benefit of power conservation to obtain the invention as specified in claim 1.

With respect to claim 2, APA discloses, a method of driving a liquid crystal display device, the liquid crystal display device comprising driver circuit, which comprises a timing controller (110 in fig. 1) driven by a data transmission signal (LOAD signal) (fig. 2) and a source driver (120 in fig. 1) driven by a data reception signal (DSTH signal) (fig. 2).

APA does not expressly disclose, the method being characterized in that: within the period from the time when data transmission signal (LOAD signal) is enabled to the time when the data reception signal (DSTH signal) is enabled, a data clock (DCLK signal) is forced to be at a low voltage level.

Kim discloses, within the period from the time when data transmission signal (LOAD signal) (STV2 in fig. 9) is enabled to the time when the data reception signal

(DSTH signal) (STV1 in fig. 9) is enabled, a data clock (DCLK signal) (clk1 in fig. 9) is forced to be at a low voltage level (fig. 9, col. 5, lines 33-35; clk1 is at a at a high voltage between STV1 and STV2, i.e. when driving that specific gate line. Clk1 is not provided (set at a low voltage) when no driving signals are necessary for the gate, col. 5, lines 57-62, col. 6, lines 3-5).

At the time of the invention it would have been obvious to one of ordinary skill in the art to not provide a clock signal, as taught by Kim, between the LOAD and the DSTH signal of APA.

The motivation for doing so would have been to reduce unnecessary power consumption (Kim, col. 6, lines 3-5).

Therefore it would have been obvious to combine Kim with APA for the benefit of power conservation to obtain the invention as specified in claim 2.

With respect to claim 9, APA discloses, a method of driving a liquid crystal display device, the liquid crystal display device comprising driver circuit, which comprises a timing controller (110 in fig. 1) driven by a data transmission signal (LOAD signal) (fig. 2) and a source driver (120 in fig. 1) driven by a data reception signal (DSTH signal) (fig. 2), the method comprising the steps of: detecting the status of the LOAD signal to determine whether the data input begins; detecting the status of the DSTH signal to determine whether the data input is completed.

APA does not expressly disclose forcing a DCLK signal (clk1 in fig. 9) to be at a low voltage level when the LOAD signal is at a high voltage level; and returning the DCLK signal to be at a normal voltage level when the DSTH signal is detected (see the

clk1 signal in fig. 9; also see col. 5, lines 33-62 for general operation discussion that is equivalent to the claimed invention as it is presently understood).

Kim discloses, forcing a DCLK signal (clk1 in fig. 9) to be at a low voltage level when the LOAD signal is at a high voltage level (STV2 in fig. 9); and returning the DCLK signal to be at a normal voltage level when the DSTH signal is detected (see the clk1 signal in fig. 9; also see col. 5, lines 33-62 for general operation discussion that is equivalent to the claimed invention as it is presently understood).

At the time of the invention it would have obvious to one of ordinary skill in the art to not provide a clock signal, as taught by Kim, between the LOAD and the DSTH signal of APA.

The motivation for doing so would have been to reduce unnecessary power consumption (Kim, col. 6, lines 3-5).

Therefore it would have been obvious to combine Kim with APA for the benefit of power conservation to obtain the invention as specified in claim 9.

With respect to claims 3 and 10, APA further discloses, wherein the LOAD signal is enabled at a high voltage level (LOAD in fig. 2).

With respect to claim 5 and 12, Kim further discloses, wherein forcing the DCLK signal (clk1) to be at a low voltage level begins at the falling edge of the LOAD signal (STV2) when being as a high voltage level (note dashed line from the falling edge of STV2 to the turning off of clk1; col. 5, lines 33-35).

With respect to claims 6 and 13, APA further discloses, wherein the DSTH signal is enabled at a high voltage level (DSTH in fig. 2).

With respect to claims 8 and 15, Kim discloses, wherein forcing the DCLK signal (clk1) to be at a low voltage level ends at the rising edge of the DSTH signal (STV1) when being as a high voltage level (note dashed line from the rising edge of STV1 to the turning on of clk1; col. 5, lines 33-35).

6. Claims 4, 7, 11 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's own Prior Art admissions (hereafter APA) in view of Kim (US 6,414,670) and further in view of Ranganathan (US 5,615,376).

With respect to claim 4 and 11, APA and Kim disclose, the methods of claims 3 and 10 (see above).

Neither APA nor Kim expressly disclose, wherein forcing the DCLK signal to be at a low voltage level begins at the rising edge of the LOAD signal when being as a high voltage level.

Ranganathan discloses, forcing VCLK (20' in fig. 4) to be a low voltage level at the rising edge of a signal (22 in fig. 4).

Ranganathan, APA and Kim are all analogous art because they are all drawn to the same field of endeavor namely LCD control circuitry.

At the time of the invention it would have been obvious to lower the clock voltage, disclosed by Kim and APA, at the rising edge of a signal as taught by Ranganathan.

The motivation for doing so would have been to achieve clock lowering more quickly, thus conserving more power.

Therefore it would have been obvious to combine Ranganathan with Kim and APA for the benefit of power conservation to obtain the invention as specified in claims 4 and 11.

With respect to claims 7 and 14, APA and Kim disclose, the methods of claims 6 and 13 (see above).

Neither APA nor Kim expressly disclose, wherein forcing the DCLK signal to be at a low voltage level ends at the falling edge of the DSTH signal when being as a high voltage level.

Ranganathan discloses, ends forcing VCLK (20' in fig. 4) to be a low voltage level at the falling edge of a signal (24 in fig. 4).

At the time of the invention it would have been obvious to enable the clock voltage, disclosed by Kim and APA, at the falling edge of a signal as taught by Ranganathan.

The motivation for doing so would have been to slightly extend the clock lowering, thus conserving more power.

Therefore it would have been obvious to combine Ranganathan with Kim and APA for the benefit of power conservation to obtain the invention as specified in claims 7 and 14.

Claims 4, 7, 11 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (US 6,414,670) in view of Ranganathan (US 5,615,376).

With respect to claim 4 and 11, Kim discloses, the methods of claims 3 and 10 (see above).

Kim does not expressly disclose, wherein forcing the DCLK signal to be at a low voltage level begins at the rising edge of the LOAD signal when being as a high voltage level.

Ranganathan discloses, forcing VCLK (20' in fig. 4) to be a low voltage level at the rising edge of a signal (22 in fig. 4).

Ranganathan and Kim are all analogous art because they are all drawn to the same field of endeavor namely LCD control circuitry.

At the time of the invention it would have been obvious to lower the clock voltage, disclosed by Kim, at the rising edge of a signal as taught by Ranganathan.

The motivation for doing so would have been to achieve clock lowering more quickly, thus conserving more power.

Therefore it would have been obvious to combine Ranganathan with Kim for the benefit of power conservation to obtain the invention as specified in claims 4 and 11.

With respect to claims 7 and 14, Kim discloses, the methods of claims 6 and 13 (see above).

Kim does not expressly disclose, wherein forcing the DCLK signal to be at a low voltage level ends at the falling edge of the DSTH signal when being as a high voltage level.

Ranganathan discloses, ends forcing VCLK (20' in fig. 4) to be a low voltage level at the falling edge of a signal (24 in fig. 4).

At the time of the invention it would have been obvious to enable the clock voltage, disclosed by Kim, at the falling edge of a signal as taught by Ranganathan.

The motivation for doing so would have been to slightly extend the clock lowering, thus conserving more power.

Therefore it would have been obvious to combine Ranganathan with Kim for the benefit of power conservation to obtain the invention as specified in claims 7 and 14.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Rivera-Cintron et al. (US 2004/0119670) discloses turning an external clock on and off depending upon data reception. Specifically note figure three. Kubota et al. (US 6,437,768) discloses lowering and raising a clock voltage to conserve power (fig. 5).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Will Boddie whose telephone number is (571) 272-0666. The examiner can normally be reached on Monday through Friday, 7:30 - 4:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Edouard can be reached on (571) 272-7603. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Wlb
1/23/06

PATRICK N. EDOUARD
SUPERVISORY PATENT EXAMINER